REMARKS

Response to Arguments

The Examiner stated that the Applicant's remarks/arguments with respect to the rejections of claims 1–20 under 35 U.S.C §102 (b) have been fully considered and are persuasive. Therefore, the rejection has been withdrawn.

Claim Rejections - 35 USC §102

Claims 1-20 are rejected under 35 USC §102(b) as being anticipated by Kirsch et al. (U.S. Patent No. 6,507,933 B1, hereinafter "Kirsch").

Kirsch provides a method and system for automatic defect source classification for use in wafer fabrication quality control. The method and system make quantitative a qualitative integrated circuit wafer defect signature. In response to the quantitativized wafer fabrication defect signature, the method and system identify at least one cause of the defect signature and determine corrective action to remove the condition that caused the defect.

Summary of Applicant's Arguments

Kirsch is directed to process defect control, not to making decisions about whether to proceed with <u>further</u> processing of existing, partially completed wafer production lots, by analyzing the effects of wafer defects upon later wafer layers. Kirsch provides for analysis of defects in order to adjust currently running production and fabrication processes to reduce or eliminate further defects in <u>future</u> wafer lots. Kirsch discloses nothing about what happens to an existing production lot following Kirsch's defect analysis of that lot, i.e., whether to finish processing that wafer production lot or to abort that production lot.

Kirsch is thus directed to identifying and correcting wafer process steps to minimize the recurrence of <u>similar</u> defects in <u>later produced wafers</u>. Kirsch does not address the question of whether to proceed with further processing of <u>existing</u> intermediate wafers that already have defects.

The present invention discloses and claims methods and systems for making intelligent decisions concerning whether to proceed with further processing of partially completed wafers that have already acquired defects. As pointed out in the present application, each finished semiconductor wafer has hundreds to tens of thousands of integrated circuits ("ICs"), each worth hundreds or thousands of dollars. The decision whether or not to finish processing a partially defective wafer lot is therefore a crucially important economic decision. For example, many ICs (e.g., memory chips) with minor defects can still be perfectly serviceable because they contain redundancies allowing defective elements to be mapped out.

But it is not always readily determinable how serious an intermediate defect is, and whether the defect will be "fatal", or will cause only minor consequences.

The present invention, as disclosed and claimed, enables such "proceed or stop" decisions to be made by disclosing the future effects upon later layers of current defects.

Kirsch has no such disclosure. Kirsch does not address or facilitate subsequent proceed or stop disposition decisions.

Kirsch accordingly fails to anticipate the present invention under 35 USC §102(b). The rejection should therefore be withdrawn, the claims should be allowed, and the application should be passed to issuance.

Detailed Response to the Rejection

The independent claims 1, 6, 11, and 16 have been clarified to amend the previously claimed combination, as exemplified in claim 1, to now include the limitation of:

> "utilizing the at least one layer model to determine the subsequent disposition of the
> wafer production lot, including whether to proceed with further processing of
> the wafer production lot."

The support for the above amendment is on page 7, line 13.

Regarding claims 1, 6, 11, and 16, the Applicant respectfully traverses the rejection since the Applicant's claimed combination, as exemplified in claim 1, now includes the limitation not disclosed in Kirsch of:

"utilizing the at least one layer model to determine the subsequent disposition of the wafer production lot, including whether to proceed with further processing of the wafer production lot."

The Examiner states in the Office Action dated November 13, 2006:

"(d) utilizing the layer model to determine the subsequent disposition of the wafer production lot (see again col. 2, II. 3 - 50; col. [sic])."

However, Kirsch does not disclose utilizing the layer model to determine whether to proceed with further processing of the wafer production lot. Instead, at col. 2, lines 3–50, Kirsch states:

"Dispositioning...entails...(4) if a determination is made that the defect map of the wafer represents significant defects in the manufacture of the wafer, determining one or more likely "causes" of the significant defects...
...
There are several problems associated with dispositioning...as follows...to recognize certain visual patterns (known in the art as "defect signatures") in defect maps, and associate those certain patterns with specific "causes" of the defects within the production process of the integrated circuit wafers..."[deletions for clarity]

Thus Kirsch does not disclose utilizing the layer model to determine whether to proceed with further processing of the wafer production lot as claimed in claims 1, 6, 11, and 16.

Regarding claims 1, 6, 11, and 16, the Applicant also respectfully traverses the rejection since the Applicant's claimed combination, as exemplified in claim 1, includes the limitation not disclosed in Kirsch of:

"generating at least one layer model from the information and data to disclose the effects of the at least one defect upon at least one later layer of the semiconductor wafer"

The Examiner states in the Office Action dated November 13, 2006:

"(c) generating at least one layer model from the information and data to disclose the effects of the defect upon at least one later layer of the semiconductor layer (see col. 2, II.3 - 22; col. 2, II. 35 -41)"

However, Kirsch does not disclose disclosing the effects of the defect upon a <u>later</u> layer of the semiconductor wafer. Instead, at col. 2, lines 3–22 and lines 35–41, Kirsch states:

"Dispositioning...entails...(4) if a determination is made that the defect map of the wafer represents significant defects in the manufacture of the wafer, determining one or more likely "causes" of the significant defects, where the determination of the "cause" encompasses both (a) where the defect occurred...and (b) why the defect occurred..." [deletions for clarity]

"This training typically involves teaching the prospective dispositioner to recognize certain visual patterns...in defect maps, and associate those certain patterns with specific "causes" of the defects within the production process of the integrated circuit wafers. Second, being human, dispositioners are tremendously variable, with some being markedly better than others." [deletions for clarity]

This disclosure is a retrospective analysis of what caused the defect, not a forward-looking prediction of the effects of the defect on later layers. Thus Kirsch does not disclose disclosing the effects of the defect upon a later layer of the semiconductor wafer as claimed in claims 1, 6, 11, and 16.

Based on the above, it is respectfully submitted that independent claims 1, 6, 11, and 16, and the respective claims 2–5, 7–10, 12–15, and 17–20 depending therefrom, are allowable under 35 USC §102(b) because:

"Anticipation requires the disclosure in a single prior art reference disclosure of each and every element of the claim under consideration." W.L. Gore & Assocs. v. Garlock, Inc., 721 F.2d 1540, 220 USPQ 303, 313 (Fed. Cir. 1983) (citing Soundscriber Corp. v. United States, 360 F.2d 954, 960, 148 USPQ 298, 301 (Ct. Cl.), adopted, 149 USPQ 640 (Ct. Cl. 1966)), cert. denied, 469 U.S. 851 (1984). Carella v. Starlight Archery, 804 F.2d 135, 138, 231 USPQ 644, 646 (Fed. Cir.), modified on reh'g, 1 USPQ 2d 1209 (Fed. Cir. 1986); RCA Corp. v. Applied Digital Data Sys., Inc., 730 F.2d 1440, 1444, 221 USPQ 385, 388 (Fed. Cir. 1984).

Withdrawal of the rejection is therefore respectfully requested.

Regarding claims 2, 3, 7, 8, 12, 13, 17, and 18, these dependent claims each depend from respective independent claims 1, 6, 11, and 16, and are believed to be allowable since they contain all the limitations set forth in the independent claims from which they depend and additionally claim non-obvious combinations thereof. Allowance of claims 2, 3, 7, 8, 12, 13, 17, and 18 is therefore respectfully requested because of W.L. Gore & Assocs. v. Garlock, Inc. and the other cases cited therewith, supra.

The Applicant also respectfully traverses the rejection of claims 2, 3, 7, 8, 12, 13, 17, and 18 since the Applicant's claimed combination, as exemplified respectively in claims 2 and 3, includes the respective limitations not disclosed in Kirsch of:

"disclosing the components that will be located above the at least one defect in the semiconductor wafers" (claim 2)

and

"treating the data concerning the at least one defect as a new layer of information" (claim 3)

The Examiner states in the Office Action:

"Pursuant to claims 2 and 3 see col. 2, ll. 31 - 40; col. 2, ll. 59 - 67; col. 5, ll. 1 - 30, which suggest the limitations pertaining to generating and utilizing a layer model (i.e., defect signature) to determine subsequent disposition of the wafer production lot (claim 3), and suggesting the locations of components above a defect in a wafer (claim 2)."

However, Kirsch does not disclose disclosing the components that will be located above the at least one defect in the semiconductor wafers (claim 2) or treating the data concerning the at least one defect as a new layer of information (claim 3). Instead, in the sections cited by the Examiner (quoted and identified below), Kirsch merely states:

"There are several problems associated with dispositioning...First, it takes roughly 6 months to 2 years to adequately train a human to do dispositioning. This training typically involves teaching the prospective dispositioner to recognize certain visual patterns...in defect maps, and associate those certain patterns with specific "causes" of the defects within the production process of the integrated circuit wafers." (col. 2, lines 31 – 40) [deletions for clarity]

"A method and system have been invented which will automatically perform the functions currently performed by the human dispositioners...The method and system quantitativize[1] a qualitative integrated circuit wafer defect signature. In response to the quantitativized wafer fabrication defect signature, the method and system identify at least one cause of the defect signature." (col. 2, lines 59 – 67) [deletions for clarity]

"Once a lot is placed on hold, a sampling of the defects (typically 50 defects per wafer) must be reviewed and classified...The dispositioner must then take the wafer map and defect types and then determine the source of the defects, and the corrective action. In most cases, the pattern of defects on the wafer map and the types of defects on the wafer are unique for a specific

problem of a specific process tool. This combination of defect map pattern and defect types is known in the industry as a process signature.

Subsequent to the production of defect map 304, human dispositioner 306 visually inspects 308 defect map 304 and determines whether a significant defect pattern is indicated by defect map 304...In the event that a significant defect pattern is indicated by defect map 304, human dispositioner 306 then in response the morphology...of defect pattern 304 (a) posits 310 one or more points in the process of producing the wafer where the significant defect pattern might have arisen, and (b) for each posited one or more points in the process wherein the defect pattern might have arisen, posits 312 one or more events or conditions which might have caused the defect patterns to arise." (col. 5, lines 1 – 30) [deletions for clarity]

Thus, Kirsch discloses searching for the source of particular defects and identifying the source(s) of the defect. The search may span different process steps, but that is not the same as disclosing the components that will be located above the at least one defect in the semiconductor wafers (claim 2) or treating the data concerning the at least one defect as a new layer of information (claim 3).

Accordingly, Kirsch makes no reference to nor discloses disclosing the components that will be located above the at least one defect in the semiconductor wafers (claims 2, 7, 12, and 17) or treating the data concerning the at least one defect as a new layer of information (claims 3, 8, 13, and 18), as claimed. Allowance of claims 2, 3, 7, 8, 12, 13, 17, and 18 is therefore respectfully requested on this ground as well because of W.L. Gore & Assocs. v. Garlock, Inc. and the other cases cited therewith, *supra.*

Regarding claims 4, 9, 14, and 19, these dependent claims depend from respective independent claims 1, 6, 11, and 16, and are believed to be allowable since they contain all the limitations set forth in the respective independent claims from which they depend and additionally claim non-obvious combinations thereof. Allowance of claims 4, 9, 14, and 19 is therefore respectfully requested because of W.L. Gore & Assocs. v. Garlock, Inc. and the other cases cited therewith, *supra.*

The Applicant also respectfully traverses the rejection of claims 4, 9, 14, and 19 since the Applicant's claimed combination, as exemplified in claim 4, includes the limitation not disclosed in Kirsch of:

"determining whether the at least one defect would be likely to cause at least one of: bridging at a subsequent layer, an open circuit, blockage at a later layer, and blockage between layers"

The Examiner states in the Office Action:

"As for claim 4, see items (4) and (5) above, as well as col. 4, ll. 44 - 67, which cite the likely cause and clustering of possible defects in a production wafer lot, as claimed."

However, Kirsch makes no reference to nor discloses bridging, an open circuit, or blockage, <u>at a subsequent layer</u> as claimed in claims 4, 9, 14, and 19. Allowance of claims 4, 9, 14, and 19 is therefore respectfully requested on this ground as well because of W.L. Gore & Assocs. v. Garlock, Inc. and the other cases cited therewith, *supra.*

Regarding claims 5, 10, 15, and 20, these dependent claims depend from respective independent claims 1, 6, 11, and 16, and are believed to be allowable since they contain all the limitations set forth in the respective independent claims from which they depend and additionally claim non-obvious combinations thereof. Allowance of claims 5, 10, 15, and 20 is therefore respectfully requested because of W.L. Gore & Assocs. v. Garlock, Inc. and the other cases cited therewith, *supra.*

It is therefore respectfully submitted that independent claims 1, 6, 11, and 16, and the respective claims 2–5, 7–10, 12–15, and 17–20 depending therefrom, are allowable under 35 USC §102(b). Allowance of claims 1–20 is therefore respectfully requested because of W.L. Gore & Assocs. v. Garlock, Inc. and the other cases cited therewith, *supra.*

Conclusion

In view of the above, it is submitted that the claims are in condition for allowance and reconsideration of the rejections is respectfully requested. Allowance of claims 1–20 at an early date is solicited.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this

paper, including any extension of time fees, to Deposit Account No. 01-0365 and please credit any excess fees to such deposit account.

Respectfully submitted,

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